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Patent

Attorney Docket: 264/087

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of:

Takahide Ohkami

Serial No.: 09/879,658

Filed: June 11, 2001

For: Hardware-Assisted Design Verification
System Using A Packet-Based Protocol Logic
Synthesized For Efficient Data Loading and
Unloading

) Group Art Unit: 2123

) Examiner: Not Yet Assigned

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JUL 23 2002

Technology Center 2100

REQUEST FOR CORRECTED FILING RECEIPT
DUE TO PATENT AND TRADEMARK OFFICE ERROR

Assistant Commissioner For Patents
Washington, D.C. 20231

Sir:

On June 11, 2001, Applicant filed with the United States Patent and Trademark Office the above-identified application. Attached hereto as Exhibit A is a copy of the New Application Transmittal reflecting the title of the invention to read: "Hardware-Assisted Design Verification System Using A Packet-Based Protocol Logic Synthesized For Efficient Data Loading and Unloading".

CERTIFICATE OF MAILING
(37 C.F.R. §1.8a)

I hereby certify that this paper (along with any referred to as being attached or enclosed) is being deposited with the United States Postal Service on the date shown below with sufficient postage as First Class Mail in an envelope addressed to the Assistant Commissioner for Patents, Washington, D.C. 20231.

Jeffrey A. Miller

Name of Person Mailing Paper

July 1, 2002
Date of Deposit

Signature of Person Mailing Paper

Patent
Attorney Docket: 264/087

Attached hereto as Exhibit B is the filing receipt reflecting a typographical error in the title.

"Hardware-assisted disign ..." should read "Hardware assisted design ...".

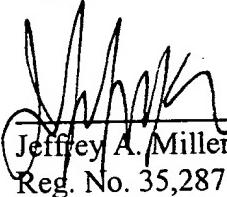
Applicant respectfully requests that a Corrected Filing Receipt be issued reflecting the correct spelling of the title and that the correction also be made to the electronic publication published on April 25, 2002.

The Commissioner is authorized to charge any fees required by the filing of this paper, and to credit any overpayment to Lyon & Lyon's Deposit Account No. 12-2475.

Respectfully submitted,

LYON & LYON LLP

By:


Jeffrey A. Miller
Reg. No. 35,287

Dated: July 1, 2002

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UNITED STATES PATENT AND TRADEMARK OFFICE

COMMISSIONER FOR PATENTS
 UNITED STATES PATENT AND TRADEMARK OFFICE
 WASHINGTON, D.C. 20231
www.uspto.gov

APPLICATION NUMBER	FILING DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	DRAWINGS	TOT CLAIMS	IND CLAIMS
09/879,658	06/11/2001	2123	840	264/087	18	10	3

22249
 LYON & LYON LLP
 633 WEST FIFTH STREET
 SUITE 4700
 LOS ANGELES, CA 90071



COPY OF PAPERS
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CONFIRMATION NO. 2956

UPDATED FILING RECEIPT



OC00000000699508

Date Mailed: 10/30/2001

Receipt is acknowledged of this nonprovisional Patent Application. It will be considered in its order and you will be notified as to the results of the examination. Be sure to provide the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION when inquiring about this application. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. If an error is noted on this Filing Receipt, please write to the Office of Initial Patent Examination's Customer Service Center. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections (if appropriate).

Applicant(s)

Takahide Ohkami, Newton, MA;

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Assignment For Published Patent Application

Quickturn Design Systems, Inc.;

JUL 23 2002

Technology Center 2100

Domestic Priority data as claimed by applicant

THIS APPLN CLAIMS BENEFIT OF 60/242,407 10/20/2000

Foreign Applications

If Required, Foreign Filing License Granted 08/15/2001

Projected Publication Date: 04/25/2002

Non-Publication Request: No

R E C E I V E D

Early Publication Request: No

NOV 02 2001

U.S. PROSECUTION

Title

Hardware-assisted design verification system using a packet-based protocol logic synthesized for efficient data loading and unloading

Patent
Attorney Docket: 264/087

To: Commissioner for Patents
Box Patent Application
Washington, D.C. 20231



EL659444725US

NEW APPLICATION TRANSMITTAL - UTILITY

Sir:

Transmitted herewith for filing is a **utility** patent application:

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JUL 23 2002

Technology Center 21
2002

Inventor(s): Takahide Ohkami

Title: ~~Hardware-Assisted Design Verification System Using A Packet-Based Protocol Logic Synthesized For Efficient Data Loading and Unloading~~

I. PAPERS ENCLOSED HEREWITH FOR FILING UNDER 37 CFR § 1.53(b):

- 38 Page(s) of Written Description
4 Page(s) Claims
1 Page(s) Abstract
18 Sheets of Drawings Informal Formal

II. ADDITIONAL PAPERS ENCLOSED IN CONNECTION WITH THIS FILING:

- Declaration
 Power of Attorney Separate Combined with Declaration
 Assignment to _____ and assignment cover sheet
 Certified Copy of Priority Document No(s):
 Information Disclosure Statement w/PTO 1449 Copy of Citations
 Preliminary Amendment
 Request and Certification under 35 U.S.C. § 122(b)(2)(B)(i). Applicant must attach form PTO/SB/35
 Return Postcard
 Other:

III. PRIORITY

- Priority of application Serial No. 60/242,407 filed on October 20, 2000 in the United States is claimed under 35 U.S.C. § 119.

2FC1



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 WASHINGTON, D.C. 20231
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Bib Data Sheet

SERIAL NUMBER 09/879,658	FILING DATE 06/11/2001 RULE	CLASS 703	GROUP ART UNIT 2123	ATTORNEY DOCKET NO. 264/087
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APPLICANTS

Takahide Ohkami, Newton, MA;

#4

**** CONTINUING DATA *******

THIS APPLN CLAIMS BENEFIT OF 60/242,407 10/20/2000

**** FOREIGN APPLICATIONS *********IF REQUIRED, FOREIGN FILING LICENSE GRANTED**

** 08/15/2001

Foreign Priority claimed	<input type="checkbox"/> yes <input type="checkbox"/> no	STATE OR COUNTRY	SHEETS DRAWING	TOTAL CLAIMS	INDEPENDENT CLAIMS
35 USC 119 (a-d) conditions met	<input type="checkbox"/> yes <input type="checkbox"/> no <input type="checkbox"/> Met after Allowance	MA	18	10	3
Verified and Acknowledged	Examiner's Signature _____ Initials _____				

ADDRESS

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TITLE

Hardware-assisted design verification system using a packet-based protocol logic synthesized for efficient data loading and unloading

FILING FEE RECEIVED 840	<p>FEES: Authority has been given in Paper No. _____ to charge/credit DEPOSIT ACCOUNT No. _____ for following:</p>	<input type="checkbox"/> All Fees <input type="checkbox"/> 1.16 Fees (Filing) <input type="checkbox"/> 1.17 Fees (Processing Ext. of time) <input type="checkbox"/> 1.18 Fees (Issue) <input type="checkbox"/> Other _____ <input type="checkbox"/> Credit
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